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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

TRA, TUYEN Q

ART UNIT PAPER NUMBER

2873

DATE MAILED: 11/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/715,867

Applicant(s)

WANG ET AL.

Examiner

Tuyen Q Tra

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 13 September 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-14 and 16-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-14 and 16-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

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### DETAILED ACTION

1. Applicant's arguments with respect to claims 2-14, 16-19 have been considered but are moot in view of the new ground(s) of rejection.

#### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 16 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "a first dielectric material layer underneath the electro-optic material and second dielectric layer above the electro-optic material", does not reasonably provide enablement for "a first mirror underneath the electro-optic material and a second mirror above the electro-optic material forming a cavity". The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims.

The specification does not disclose a first and a second mirrors are separated from a first and second dielectric layers or how the second mirror is formed.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 16 directed to a device can be read to include the same element (dielectric material is a dielectric layer and a mirror) twice. See MPEP 2173.05(o).

Claims 2-14, 17-19 are rejected because of depending on the claim 16.

*Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 16, 6, 12 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Tayebati et al. (U.S. Pat. 6,025,950 A).

a) With respect to claim 16, Tayebati et al. discloses a spatial light modulator in Fig. 4 and 7 comprising of:

an array of pixels formed on a semiconductor substrate (225), each pixel including a solid state electro-optic material (215) positioned between a first and a second electrode (205);

a first electrode underneath the electro-optic material and a second electrode (205) above the electro-optic material (215) forming a cavity;

a first mirror (220) underneath the electro-optic material (215), and second mirror formed by electrode layer (205) and dielectric layer (210) above the electro-optic material (215) to form a cavity.

an array of pixel circuits formed with the semiconductor substrate, each pixel being connected to a pixel circuit (see Fig. 4).

b) With respect to claim 6, Tayebati et al. further discloses the electro-optic material comprising of plurality of layers (215).

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c) With respect to claim 12, Tayebati et al. further discloses a first electro-optic layer comprising a first electro-optic layer (215, top) and additional layers (215, followed top layer) comprising a second electro-optic material (see Fig. 7).

d) With respect to claims 17, Tayebati et al. further discloses the first and second layer of dielectric material each comprises a stack of dielectric thin film.

*Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 4, 8, 10, 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tayebati et al. (U.S. Pat. 6,025,950 A), as applied to claim 16 above, in view of Robinson et al. (U.S. Pat. 6,091,463 A).

Tayebati et al. discloses spatial light modulator device with an array of pixel circuits formed with the semiconductor substrate, each pixel being connected to a pixel circuit. However, Tayebati et al. does not teach the pixel circuit comprising of an array of transistors formed on a silicon substrate; the semiconductor comprises a CMOS integrated circuit; a memory circuit collocated with each pixel; and each pixel circuit comprises a RAM; a copper interconnect along a mesa sidewall to a circuit contact of a pixel circuit. Within the same field of endeavor, Robinson et al. discloses a diffractive spatial light modulator comprises pixel circuits comprising of an array of transistors formed on a silicon substrate (col. 4, lines 20-29, Fig. 2); the semiconductor comprises a CMOS integrated circuit (col. 2, lines 38-41), a memory circuit

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collocated with each pixel, and each pixel circuit comprises a RAM; a copper interconnect along a mesa sidewall to a circuit contact of a pixel circuit (col. 4, lines 33-40).

It would have been obvious, therefore, at the time the invention was made to a person having skill in the art to construct a spatial light modulator with array of pixel circuit such as disclosed by Tayebati et al. with an array of transistors formed on a silicon substrate; the semiconductor comprises a CMOS integrated circuit; a memory circuit collocated with each pixel; and each pixel circuit comprises a RAM; a copper interconnect along a mesa sidewall to a circuit contact of a pixel circuit such as discloses by Robinson et al., for purpose of controlling optical device electronically.

9. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tayebati et al. (U.S. Pat. 6,025,950 A), as applied to claim 12.

Tayebati et al. discloses a spatial light modulator and method comprising of an electro-optic material. However, Tayebati et al. does not implicitly disclose that the electro-optic material comprising of PLZT.

The selection of PLZT material in place of electro-optic is seem as design experience upon the environment of use to ensure optimum performance. In addition, the applicant has presented no discussion in the specification that convinces examiner that the particular electrooptic material could produce functional different or obvious results. Therefore, it would have been obvious at the time invention was made to a person having skill in the art to use PLZT material in stead for mater of design choice.

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10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tayebati et al. (U.S. Pat. 6,025,950 A), as applied to claim 16, in view of Birnbach et al. (U.S. Pat. 4,786,128).

Tayebati et al. discloses a spatial light modulator and method comprising of electro-optic material layer, first and second electrodes. However, Tayebati et al. fails to teach first and second electrodes comprises of an optically transmissive conductive material. Within the same field of endeavor, Birnbach discloses a spatial light modulator with electrodes 14 and 16 comprise of layer L1 and L2 are optically transmissive conductive material (col. 5, line 1-3).

It would have been obvious, therefore, at the time the invention was made to a person having skill in the art to construct a spatial light modulator with a first and second electrodes such as disclosed by Tayebati et al., with first and second electrodes material comprising of an optically transmissive conductive material such as discloses by Birnbach, for purpose of transmitting light to mirror.

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tayebati et al. (U.S. Pat. 6,025,950 A), as applied to claim 16, in view of Bowman et al. (U.S. Pat. 5,637,883).

Tayebati et al. discloses a spatial light modulator and method comprising of electrode layers. However, Tayebati et al. does not implicitly disclose that the electrode layers comprises of an electrically conductive layer that contacts a dielectric layer. Within the same field of invention, Bowman et al. discloses a spatial light modulator comprises an electrode layer comprising of an electrically conductive layer 28 that contacts a dielectric layer 26 (see Fig. 1).

It would have been obvious, therefore, at the time the invention was made to a person having skill in the art to construct a spatial light modulator with electrode layers such as

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disclosed by Tayebati et al., with an electrode layer comprising of an electrically conductive layer 28 that contacts a dielectric layer 26 such as discloses by Bowman et al., for purpose of forming a mirror layer in spatial light modulator.

12. Claims 2, 3, 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tayebati et al. (U.S. Pat. 6,025,950 A), as applied to claim 16, in view of Gobeli (U.S. Pat. 5,768,003).

a) With respect to claim 2, 5 and 9, Tayebati et al. discloses an optical device but fails to implicitly disclose solid-state electro-optic material comprising of ceramic material; electro-optic layer having thickness less than 2000nm; a light source and an optical coupler. Within the same field of endeavor, Gobeli further discloses solid-state electro-optic material 10A comprising of ceramic material (i.e. PLZT) (col. 3, line 65); electro-optic material layer having thickness of 15 nm (col. 3, lines 31-32); a light source and an optical coupler (col. 6, line 46-47).

It would have been obvious, therefore, at the time the invention was made to a person having skill in the art to construct a spatial light modulator with electrode layers such as disclosed by Tayebati et al., with solid-state electro-optic material 10A comprising of ceramic material; electro-optic material layer having thickness of 15 nm; a light source and an optical coupler such as discloses by Gobeli for purpose of providing and focusing light to the modulator.

b) With respect to claim 3, Gobeli discloses a spatial light modulator with solid-state electro-optic layers (10A) comprising of PLZT. However, Gobeli does not implicitly disclose the solid-state electro-optic material layer (10A) comprising of ceramic material.



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The selection of ceramic material in place of PLZT is seen as design experience upon the environment of use to ensure optimum performance. In addition, the applicant has presented no discussion in the specification that convinces examiner that the particular ceramic material could produce functional different or obvious results. Therefore, it would have been obvious at the time invention was made to a person having skill in the art to use ceramic material in stead for mater of design choice.

### *Conclusion*

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a) Patel (US Pat. 5,068,749) discloses an optical filter with mirrors (32, 34), electro-optic material (36), and dielectric material (20, 22).
- b) McMurray (US Pat. 4,925,276) discloses liquid crystal valve with electro-optic effect.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen Tra whose telephone number is (703) 306-5712. The examiner can normally be reached on Monday to Friday from 8:30am to 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps, can be reached on (703) 308-4883. The fax number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Examiner: Tuyen Tra

Date: November 20, 2002

  
Hung Xuan Dang  
Primary Examiner